Accelerate real-time high definition video processing designs with Digilent Zybo Z7, a Zynq-7000 AP SoC Platform and Xilinx Vivado HLS

Goals:

- Show how to use High Level Synthesis (HLS) to configure the field programmable gate array (FPGA)
- Explain how to build the real-time video processing pipelines and Intellectual Property (IP) in the Xilinx computer aided design (CAD) tool.
- Illustrate the viability of real-time video processing in reconfigurable logic instead of software running on a general-purpose microprocessor.

Description:

The workshop aligns with Digilent's mission of providing a hands-on, project-based, open-ended approach to education. Attendees will use Digilent Zybo Z7 (*a Xilinx Zynq SoC FPGA platform)*, PCAM (*5MP camera sensor)* and Xilinx Vivado HLx to implement a real-time high definition video processing application.
Examples in the workshop materials are based on both high-level programming language (C++) and hardware description language (VHDL). Trainers will demonstrate HLS design flow, IP core usage, simulation and hardware debugging. Participants will leave the workshop with instructional materials and PCAM, 5MP camera sensor so that they can easily adopt this innovative technique in their own courses and projects. \

What you need to prepare

- Please bring a laptop with
    - Windows 7 at minimum (limited Linux support available)
    - Vivado 2018.1 Design Suite (including Vivado HLS and SDK) installed and licensed (WebPack at least)

Format: Hands-on tutorial in English

List of Topics covered:

- Explain parallelism and program execution
- Introduce Xilinx FPGA Architecture and Vivado HLS
- Introduce Digilent Zybo Z7 and PCAM
- Accelerate video processing algorithm on Xilinx Vivado
- Implement video processing design on Digilent Zybo Z7 and PCAM

Target Audience:

The anticipated audience includes faculty members, instructors, laboratory staff, graduate students in the Electrical and Computer Engineering department. Participants need to have basic knowledge about VHDL, C/C++ and digital design.

Speakers:

- Arthur Brown, *Digilent Inc*

Arthur Brown is an enthusiastic Digital Design Engineer with experience in Xilinx FPGA and embedded software development. He has been running HLS workshops across Europe.