

Call For Participation

FPT'18

International Conference on Field-programmable Technology
Dec 10-14, 2018, Naha, Okinawa, Japan

Online Registration Due: Nov 25

<http://www.fpt18.sakura.ne.jp>



Program: Technical Sessions, Keynote/Invited Talks,
Workshops, and Design Contest



Dec 12

Keynote Speaker

Hideharu Amano

Keio University, Professor

“Accelerator-in-Switch:
a novel cooperation
framework for FPGAs and
GPUs”



Dec 13

Keynote Speaker

Mike Strickland

Intel PSG, Director

“FPGA Accelerated HPC
and Data Analytics”



Dec 13

Invited Speaker

Hiroshi Miyata

Fujitsu Laboratories Ltd., Fellow

“Digital Transformation of
Automobile and Mobility
Service”



Dec 14

Keynote Speaker

Kees Vissers

Xilinx, Fellow

“Novel Neural Network
Applications on New Python
Enabled Platforms”

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PASONA

TECH DENSO

Crafting the Core

TOKYO ELECTRON DEVICE

Bronze

HUMANDATA.



Program

10 Dec. (Mon)		11 Dec. (Tue)	
10:00	Workshop PYNQ: Python productivity for Zynq	10:00 am	Workshop on Xilinx AWS
17:30		17:30	Workshop on Integrating HPC and FPGAs Workshop on Reconfigurable High-Performance Computing Workshop title: Intel OpenVINO Toolkit tutorial
12 Dec. (Wed)		13 Dec. (Thu)	
09:20	Opening	09:20	Keynote #2 (Mike Strickland)
09:40	Keynote #1 (Hideharu Amano)	10:10	Break
10:30	Break	10:40	Oral Session #4 (Design Methodologies and Tools)
11:00	Oral Session #1 (Neural Networks)	11:40	Invited Talk (Hiroshi Miyata)
12:20	Lunch & Poster Session #1 Design Competition (Preliminary) FPGA DESIGN Competition: "Autonomous Vehicle Driving Competition using FPGA"	12:20	Lunch & Poster Session #2
14:00	Oral Session #2 (High Level Synthesis)	14:00	Oral Session #5 (Networking and Data Applications)
15:40	Break	15:40	Break
16:10	Oral Session #3 (Stream Processing)	16:10	Oral Session #6 (Security and Dependability)
17:30		17:30	
18:00	Welcome Reception Ph.D / Demo Session Design Compe (Final)	19:00	Banquet
19:00		21:00	
14 Dec. (Fri)			
09:20	Keynote #3 (Kees Vissers)	09:20	
10:10	Poster Session #3	10:10	
11:00	Oral Session #7 (FPGA Architectures)	11:00	
12:00	Closing	12:00	
12:20	Lunch	12:20	
14:00	Workshop Accelerate real-time high definition video processing designs with Diligent Zybo Z7, a Zynq-7000 AP SoC Platform and Xilinx Vivado HLS	14:00	
17:30	Embedded Machine Learning: Technology and Opportunities	17:30	

More details <http://www.fpt18.sakura.ne.jp/program.html>



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	Yasunori Osana	University of Ryukyus, Japan	Design competition chair	Minoru Watanabe	Shizuoka University, Japan
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